Docket No.

FILED:

217804US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Sanae ITO, et al.

SERIAL NO: **New Application**

GAU: Herewith **EXAMINER:**

SIMULATION METHOD, SIMULATION PROGRAM, AND SEMICONDUCTOR DEVICE MANUFACTURING FOR:

METHOD EACH EMPLOYING BOUNDARY CONDITIONS

INFORMATION DISCLOSURE/RELATED CASE STATEMENT UNDER 37 CFR 1.97

ASSISTANT COMMISSIONER FOR PATENTS WASHINGTON, D.C. 20231

Applicant(s) wish to disclose the following information.

REFERENCES

- The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

- Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

- Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

Please charge any additional fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND, MAIER & NEUSTADT, P.C.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Sanae ITO, et al.

SERIAL NO.: New Application

FILED: Herewith

FOR: SIMULATION METHOD, SIMULATION PROGRAM, AND SEMICONDUCTOR

DEVICE MANUFACTURING METHOD EACH EMPLOYING BOUNDARY

CONDITIONS

STATEMENT OF RELEVANCY

Reference AO (2000-267890) of Form PTO-1449.

Simulated results are graphically shown to users interactively so that users can see the dependence of input parameters on results.

Reference AP (11-176707) of Form PTO-1449.

Calculated results and predicted their error are shown to users using information DB of differences between simulated values and measured values, so that even untrained users can do simulation without making mistake.

Reference AQ (2-222159) of Form PTO-1449.

Error correction method to the boundary condition effects for numerical capacitance calculation of periodically placed interconnect line pattern.



NAME	Form PTO 1449 (Modified)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 217804US2		SERIAL NO. New Application		
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AS AT	AQ	2-222159 09/04/90	Japan (with English abstract)			X	
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	AS						
	AT						
AU	AU						
AV	AV						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
"TWO-DIMENSIONAL PROCESS SIMULATION PROGRAM", Avant!, TSUPREM-4, User's Manual, Version 1999.2 AW 1999, (5 pages)	AW	"TWO-DIMENSIONAL PROCESS SIMULATION PROGRAM", Avant!, TSUPREM-4, User's Manual, Version 1999.2, June 1999, (5 pages)					
"TWO-DIMENSIONAL DEVICE SIMULATION PROGRAM", Avant MEDICI, User's Manual, Version 1999.2, July 199 pages)	AX	"TWO-DIMENSIONAL DEVICE SIMULATION PROGRAM", Avant MEDICI, User's Manual, Version 1999.2, July 1999, (4 pages)					
Naoyuki SHIGYO, et al., "THE INFLUENCE OF BOUNDARY LOCATIONS ON WIRING CAPACITANCE SIMULATI IEEE Transactions on Electron Devices, Vol. 36, No. 6, June 1989, pgs. 1171 - 1174.	AY	Naoyuki SHIGYO, et al., "THE INFLUENCE OF BOUNDARY LOCATIONS ON WIRING CAPACITANCE SIMULATION", IEEE Transactions on Electron Devices, Vol. 36, No. 6, June 1989, pgs. 1171 - 1174.					
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Examiner Date Considered	Examiner			Date Considered			
Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							